POLISHING APPARATUS AND METHOD FOR FORMING AN INTEGRATED CIRCUIT

Field of the Invention

The present invention relates to integrated circuit fabrication, and more specifically to a polishing apparatus and to a method for polishing a layer of material in an integrated circuit.

Background of the Invention

Polishing processes, and more specifically chemical-mechanical polishing processes, have been used in the semiconductor industry to prepare both single crystal substrates and silicon on insulator substrates. In addition, chemical-mechanical polishing processes have also been used to planarize various conductive and insulating layers subsequently deposited on these substrates, during the integrated circuit fabrication process. For example, chemical-mechanical polishing has been used to planarize interlevel dielectric layers that lie in between two different levels of metal interconnect. Planarizing the interlevel dielectric layer, prior to the formation of the next level of interconnect, is highly desirable because it allows the next level of interconnect to be subsequently patterned and etched without the formation of conductive metal stringers, which can

located near the edge of the semiconductor substrate are lost. These die represent a substantial revenue loss to integrated circuit manufactures.

Accordingly, a need exists for a polishing process and polishing apparatus that can polish semiconductor substrates with improved center to edge uniformity.

Brief Description of the Drawings

The present invention may be more fully understood by a description of certain preferred embodiments in conjunction with the attached drawings in which:

FIG. 1 illustrates, in cross-section, a polishing apparatus in accordance with one embodiment of the present invention;

FIG. 2 illustrates, in plan view, the polishing apparatus of FIG. 1;

FIG. 3 illustrates, in cross-section, a polishing apparatus in accordance with another embodiment of the present invention;

FIG. 4 illustrates, in cross-section, a polishing apparatus in accordance with another embodiment of the present invention;

FIG. 5 illustrates, in cross-section, a polishing apparatus in accordance with another embodiment of the present invention;

since the semiconductor substrate is polished with improved center to edge uniformity, die yield is increased because die located at the edge of the semiconductor substrate are not over polished.

FIG. 1 illustrates, in cross section, a polishing apparatus 5 in accordance with one embodiment of the present invention. In this particular embodiment, polishing apparatus 5 comprises a polishing platen 2, an under pad 4, a polishing pad 6, a carrier 8, and a slurry dispenser 10. In an alternative embodiment, under pad 4 is not placed between polishing pad 6 and polishing platen 2. In one embodiment, under pad 4 is a felt based under pad comprising polyurethane. For example, under pad 4 may be a SUBA IV under pad which is commercially available from RODEL, Inc.. Polishing pad 6 comprises a central region 12 having a front surface 14, and a peripheral region 16 having a front surface 18. Front surface 18 lies below front surface 14, as shown in FIG. 1. In this particular embodiment, peripheral region 16 comprises a tapered region 20 having a constant angle taper which starts at the perimeter 22 of polishing pad 6 and extends to a predetermined location 24 offset from the center 26 of polishing pad 6. It should be appreciated, that tapered region 20 may also be formed using a variable angle taper. In one embodiment, polishing pad 6 is made of a material comprising polyurethane. It should be appreciated that polishing pad 6 and under pad 4 may be formed as separate pads, or as a composite pad.

perimeter 32 of semiconductor substrate 28 remains over peripheral portion 16 while semiconductor substrate 28 is polished.

FIG. 2 illustrates, in plan view, polishing apparatus 5 of FIG. 1. Note that, carrier 8 and polishing pad 6 are illustrated as being rotated in opposite directions, and carrier 8 is illustrated as being oscillated across polishing pad 6.

FIG. 3 illustrates, in cross section, a polishing apparatus 40 in accordance with an alternative embodiment of the present invention. In this particular embodiment, polishing apparatus 40 comprises polishing platen 2, an under pad 4, a polishing pad 42, carrier 8, and slurry dispenser 10. In an alternative embodiment, under pad 4 is not placed between polishing platen 2 and polishing pad 42. Polishing pad 42 comprises a central region 44 having a front surface 46, and a peripheral region 48 having a front surface 50. Front surface 50 lies below front surface 46, as shown in FIG. 1. In this particular embodiment, peripheral region 48 comprises a tapered region 52 having a variable angle taper, and a horizontal region 54 which extends from the perimeter 56 of polishing pad 42 to tapered region 52. It should be appreciated, that tapered region 52 may also be formed using a constant angle taper. In one embodiment, polishing pad 42 is made of a material comprising polyurethane. It should be

may also be formed having horizontal holes formed within it (not shown), which extend from perimeter 76 to grooved region 72, so that slurry does not accumulate within grooved region 72 during polishing. In one embodiment, polishing pad 60 is made of a material comprising polyurethane. It should be appreciated that polishing pad 60 and under pad 4 may be formed as separate pads, or as a composite pad.

FIG. 5 illustrates, in cross section, a polishing apparatus 78 in accordance with an alternative embodiment of the present invention. In this particular embodiment, polishing apparatus 78 comprises polishing platen 2, an under pad 4, a polishing pad 80, carrier 8, and slurry dispenser 10. In an alternative embodiment, under pad 4 is not placed between polishing platen 2 and polishing pad 80. Polishing pad 80 comprises a central region 82 having a front surface 84, and a peripheral region 86 having a front surface 88. Front surface 88 lies below front surface 84, as shown in FIG. 5. In this particular embodiment, peripheral region 86 comprises a substantially vertical sidewall 90 and a horizontal region 92, which extends from the perimeter 94 of polishing pad 80 to vertical sidewall 90. In one embodiment, polishing pad 80 is made of a material comprising polyurethane. It should be appreciated that polishing pad 80 and under pad 4 may be formed as separate pads, or as a composite pad.

IC1000 polishing pad which is commercially available from RODEL, Inc.. It is important to note that polishing pad 100 conforms to the underlying topography of polishing platen 96, and therefore polishing pad 100 comprises a central region 116 having a front surface 118, and a peripheral region 120 having a front surface 122. Front surface 122 lies below front surface 118, as shown in FIG. 6. In this particular embodiment, peripheral region 120 comprises a tapered region 124 and a horizontal region 126, which extends from the perimeter 128 of polishing pad 100 to tapered region 124. It should be appreciated, however, that if polishing platen 96 is formed without horizontal region 112, as previously discussed, then tapered region 124 would start at the perimeter 128 of polishing pad 100. It should also be appreciated that polishing pad 100 and under pad 98 may be formed as separate pads, or as a composite pad.

FIG. 7 through FIG. 10 illustrate, in cross-section, process steps in accordance with one embodiment of the present invention wherein a trench isolation structure is formed in an integrated circuit. Shown in FIG. 7, is a portion 130 of an integrated circuit structure comprising a semiconductor substrate 132, a buffer layer 134, a polish-stop layer 136, and a photoresist mask 138. Semiconductor substrate 132 is preferably a monocrystalline silicon substrate. Alternatively, semiconductor substrate 132 may be a silicon-on-insulator (SOI) substrate, a silicon-on-sapphire (SOS)

using conventional photoresist stripping techniques, either before or after trenches 142 have been formed.

In FIG. 9, a dielectric layer 144 is then formed overlying semiconductor substrate 132. Dielectric layer 144 overlies pattern trench mask 140 and lies within trench 142, such that it substantially fills trenches 142 . In a preferred embodiment, dielectric layer 144 is a layer of plasma oxide, which is formed using a commercially available high density plasma deposition system. In an alternative embodiment, dielectric layer 144 is a layer of chemically vapor deposited oxide, which is deposited using ozone and tetraethylorthosilicate (TEOS) as source gases. It should be appreciated that dielectric layer 144 may also be formed using other dielectric materials, such as germanium oxide, boro-phosphate-silicate-glass (BPSG), phosphate-silicate-glass (PSG), boro-silicate-glass (BSG), spin-on-glass, or the like, and that it may be may be formed using other techniques such, electron cyclotron resonance deposition, spin-on deposition, or the like. In addition, it should also be appreciated that a trench liner (not shown) may also be formed within trenches 142 prior to forming dielectric layer 144. For example, a portion of semiconductor substrate 132 may be thermally oxidized to form a thermal oxide layer along the sidewall and bottom of trenches 142 prior to depositing dielectric layer 144. Note,

150, a dielectric layer 152, and patterned conductive members 154. Semiconductor substrate 150 is similar to semiconductor substrate 132 of FIG. 7. In one embodiment, dielectric layer 152 is a gate dielectric layer. In alternative embodiment, dielectric layer 152 is an interlevel dielectric layer. If dielectric layer 152 is a gate dielectric layer, then semiconductor substrate 150 is preferably thermally oxidized to form dielectric layer 152. It should be appreciated, however, that other dielectric materials, such as silicon oxynitride or chemical vapor deposited silicon dioxide may also be used to form a gate dielectric layer. If dielectric layer 152 is an interlevel dielectric layer then dielectric layer 152 may be a layer of silicon dioxide, a layer of silicon nitride, a layer of boro-phosphate-silicate-glass (BPSG), a layer of phosphate-silicate-glass (PSG), a layer of spin-on-glass (SOG), a silicon oxynitride layer, a polyimide layer, or the like. In addition, a combination of the foregoing dielectric materials may also be used to form dielectric layer 152. After dielectric layer 152 is formed, a conductive layer of material is formed overlying dielectric layer 152, and then patterned using conventional lithographic processes to form conductive members 154. Conductive members 154 may be formed using a doped polysilicon layer, a metal layer, a metal silicide layer, a metal nitride layer, or a combination thereof.

substrate 162 is similar to semiconductor substrate 132 of FIG. 7. In one embodiment conductive region 164 is a doped region which has been formed within a portion of semiconductor substrate 162. For example, it may be a doped source region, a doped drain region, a doped well contact, or the like. In an alternative embodiment, conductive region 164 is a patterned conductive member, such as a gate electrode, a contact plug, a via plug, an interconnect, or the like. Note, that if conductive region 164 is a gate electrode, a via plug, or an interconnect, then at least one dielectric layer (not shown) will lie between conductive region 164 and semiconductor substrate 162. Dielectric layer 166 may be a layer of silicon dioxide, a layer of silicon nitride, a layer of boro-phosphate-silicate-glass (BPSG), a layer of phosphate-silicate-glass (PSG), a layer of spin-on-glass (SOG), a silicon oxynitride layer, a polyimide layer, or the like. In addition, a combination of the foregoing dielectric materials may also be used to form dielectric layer 166. Photoresist mask 168, which overlies a portion of dielectric layer 166, is formed using standard photolithographic patterning processes.

In FIG. 15, dielectric layer 166 is etched using photoresist mask 168 to form an opening 170 within dielectric layer 166. A portion of conductive region 164 is exposed within opening 170, as shown in FIG. 15. It should be appreciated that dielectric layer 166 may be etched using a wet or a dry etch process, or a combination thereof.

abrasive. In an alternative embodiment, wherein conductive layer 174 is a copper layer and barrier layer 172 comprises tantalum, a slurry comprising hydrogen peroxide, deionized water, and a silica abrasive is used to form conductive member 176.

Thus it is apparent that there has been provided, in accordance with the present invention, a polishing apparatus and a method for polishing a layer of material in an integrated circuit that fully meets the need and advantages set forth previously. Although the invention has been described and illustrated with reference to specific embodiments thereof, it is not intended that the invention be limited to these illustrative embodiments. Those skilled in the art will recognize that modifications and variations can be made without departing from the spirit of the invention. Therefore, it is intended that this invention encompass all such variations and modifications as fall within the scope of the appended claims.